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TRANSMITTAL OF APPEAL BRIEF	Docket No. 21987-00033-US

In re Application of: Hiroyuki Inoue

Application No.	Filing Date	Examiner	Group Art Unit
09/008,497-Conf. #6301	January 16, 1998	S. H. Rao	2814

Invention: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: February 27, 2004 .

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Dated: April 28, 2004

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Docket No.: 21987-00033-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hiroyuki Inoue

Confirmation No.: 6301

Application No.: 09/008,497

Filed: January 16, 1998

Art Unit: 2814

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Examiner: S. H. Rao

APPELLANT'S BRIEF

MS Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 28, 2004

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on February 27, 2004, thus making the Appellant's Brief due on May 27, 2004, with a one (1) month extension of time. A petition for a one (1) month extension of time and deposit account authorization have been separately provided.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is: United Microelectronics Corporation, Taiwan, ROC.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 27 claims pending in this application.

B. Current Status of Claims

1. Claims canceled: 10-20, and 33

   (Claims 10-20 prosecuted in parent application, issued on April 28, 1998 as U.S. patent no. 5,744,835)

2. Claims withdrawn from consideration but not canceled: none

3. Claims pending: 1-9, 21-32, and 34-39.

4. Claims allowed: None

5. Claims rejected: 1-9, 21-32, and 34-39.

C. **Claims On Appeal:** The claims on appeal are claims 1-9, 21-32, and 34-39.

Appellant notes that claim "40", previously presented in an amendment dated March 29, 2000, should have been presented as claim "39", as no claim 39 was presented.

After revival of the application, the undersigned requested that the Examiner refer to claim "40" as "39". The results have been mixed, as the Examiner reflects claims numbered only up to "39" in the Office Action Summary and discussion of the rejections, but refers to claim 40 in the explicit statement of the rejection.

IV. STATUS OF AMENDMENTS

Appellant filed an Amendment dated October 16, 2003 in response to a non-final Official Action dated June 16, 2003 in this Continued Prosecution Application (CPA). In response to this amendment, a Final Official Action dated December 31, 2003 was mailed by the Examiner.

A Notice of Appeal was subsequently filed, with no amendments after final being presented. Accordingly, the claims enclosed herein as Appendix A do incorporate the amendments indicated in the paper filed by Appellant on October 16, 2003.

V. SUMMARY OF INVENTION

A. Introductory Remarks

This optional, introductory subsection is provided as an aid to the Examiner and the Honorable Board to provide an overview of the invention, without specific reference to Specification page and line numbers. Specific reference to page and line numbers in the Specification which provide enabling disclosure of the claimed invention, is provided in subsection "B" of this Summary of the Invention Section.

In general Appellant's disclosed and claimed invention is directed to a method for manufacturing a semiconductor device which has a buried conductive layer connected, in one embodiment, to a source or drain of a MOS transistor through a contact hole having dimensions smaller than that achievable solely by reliance upon available conventional photolithographic processing limits, i.e., "sub-photolithographic" dimensions.

Further, in view of the sub-photolithographic feature sizes achievable by the recited method, the method of Appellant's invention is designed so as to ensure that the contact hole avoids undesirable and detrimental misalignment with an associated sidewall below the contact hole, e.g., sidewalls on a gate structure, and instead generally aligns with a central portion of the device element, and avoids any overlap with the sidewall.

By avoiding alignment or registration of the contact hole with the underlying sidewall, Appellant's disclosed and recited invention solves the technical problem of damage to the silicon substrate due to exposure resulting from the undesirable alignment of the contact hole with the underlying sidewall below the contact hole. Prevention of damage to the underlying substrate, for example, is accomplished by ensuring that the contact hole is narrower than an underlying gate length, and is sufficiently centered above the gate structure so as to avoid registration or overlap with any associated sidewall underneath the contact hole.

B. Disclosure Relating to Claimed Embodiments and Aspects of the Invention

As optionally suggested by the MPEP, various embodiments and aspects of the claimed invention are discussed below with reference to page and line numbers of the Substitute Specification filed in this application by Preliminary Amendment on January 14, 1998.

In a first embodiment, a method for manufacturing a semiconductor device having a buried conductive layer which is connected to one of a source and a drain of a MOS transistor and which extends over a gate electrode of the MOS transistor comprises forming a first insulating film on a semiconductor substrate (see Specification at p. 10, lines 13-15 and FIG. 3A); forming a first conductive film as the gate electrode and a second insulating film on the first insulating film, the gate electrode having a width equal to a minimum processing size achievable with a conventional lithographic process technique (see Specification at p. 10, lines 17-28 and p. 12, lines 5-7); forming a third insulating film on the whole surface of the semiconductor substrate having the first insulating film, the first conductive film and the second insulating film formed thereon; selectively etching away the third insulating film so as to form first side wall insulating films including the third insulating film on each of both side faces of the first

conductive film and the second insulating film, the selective etching exposing the semiconductor substrate in portions which are not covered with the side wall insulating film and not covered with the first conductive film (see Specification at p. 11, lines 7-15 and FIG. 3B); diffusing impurities into the exposed portions of the semiconductor substrate so as to form a source and a drain in the semiconductor substrate (see Specification at p. 11, lines 15-20 and FIG. 3B); forming a second conductive film to be a part of the buried conductive layer on the whole surface of the semiconductor substrate having the first insulating film, the first conductive film, the second insulating film and the side wall insulating film formed thereon (see Specification at p. 11, lines 21-24 and FIG. 3C); forming a first mask layer on the second conductive film (see Specification at p. 11, lines 28-29); processing the first mask layer to have a pattern which is separated into both side portions as to the first conductive film (see Specification at p. 11, line 28 through p. 12, line 3 and FIG. 3D); forming a second mask layer on the whole surface of the semiconductor substrate having the first insulating film, the first conductive film, the second insulating film, the side wall insulating film, the second conductive film and the first mask layer formed thereon (see Specification at p. 12, lines 13-16 and FIG. 3F); selectively etching away the second mask layer so as to leave a pattern of the second mask layer as second side walls on each of both side faces of the pattern of the first mask layer (see Specification at p. 12, lines 20-22 and FIG. 3G); selectively etching away the second conductive film with the patterns of the first and second mask layers as a mask so as to process the second conductive film into a pattern in which the second conductive film is separated on the second insulating film by an opening between the second side walls smaller than the minimum processing size achievable with the conventional lithographic process technique (see Specification at least at p. 12, line 23 through p. 13, line 2; p. 18, lines 6-10), and wherein the buried conductive layer includes the second conductive film extending over the gate electrode of the MOS transistor (see Specification at p. 11, lines 21-25 and FIG. 3G); and ensuring that the opening between the second side walls does not overlap either of the first sidewall insulating films or either of the source and drain (see Specification at p. 13, lines 23-29 and FIG. 3G).

In other aspects of the claimed invention, the first mask layer is formed of an insulating film, and the second mask layer is formed of a conductive film (see Specification at p. 14, lines 1-5).

In other aspects of this embodiment, each of the first and second mask layers is formed of an insulating film, or the first mask layer may be formed of a conductive film, and the second mask layer may be formed of an insulating film, or each of the first and second mask layers may be formed of a conductive film (see Specification at p. 14, lines 1-5, and lines 21-23).

In another aspect of this embodiment, the method further comprises forming, after the step of selectively etching away the second conductive film, an interlayer insulating film on the whole surface of the semiconductor substrate having the first insulating film, the first conductive film, the second insulating film, the side wall insulating film, the second conductive film, and the first and second mask layers formed thereon; forming a contact hole through both the interlayer insulating film and the first mask layer so that the contact hole reaches the second conductive film (see Specification at p. 13, lines 4-12 and FIG. 3H); and forming a wiring layer which is connected to the second conductive film at the bottom of the contact hole (see Specification at p. 13, lines 15-20, and FIG. 3I).

In another aspect of this embodiment, the method further comprises forming, after the step of selectively etching away the second conductive film, a fourth insulating film on the whole surface of the semiconductor substrate having the first insulating film, the first conductive film, the second insulating film, the side wall insulating film, the second conductive film, and the first and second mask layers formed thereon; forming a contact hole through both the fourth insulating film and the first mask layer so that the contact hole reaches the second conductive film; forming a third conductive film in the inside of the contact hole so that the third conductive film reaches the second conductive film; processing the third conductive film into an electrode pattern; coating a surface of the third conductive film, which has been processed into the electrode pattern, with a dielectric film ; forming a fourth conductive film on the dielectric film ; and processing the fourth conductive film into an electrode pattern (see Specification at p. 15, lines 9-20, and FIG. 4).

Another aspect of this embodiment further comprises removing the first mask layer after the step of selectively etching away the second conductive film; coating at least a surface of the second conductive film with a dielectric film; forming a third conductive film on the dielectric film; and processing the third conductive film into an electrode pattern (see Specification at p. 15, line 26 through p. 16, line 8, and FIGS. 4 and 5).

In another aspect of this embodiment, a step of coating a surface of the second mask layer with a dielectric film may be included (see Specification at least at p. 15, lines 14-15, and FIG. 4), i.e., to form a capacitor and DRAM cell.

In another embodiment, a method of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size comprises forming a semiconductor element in a substrate; forming a conductive layer over the semiconductor element and the substrate; forming a first mask layer on the conductive layer; patterning the first mask layer to form a slit dividing the first mask layer into at least two mask portions, the slit having a width equal in size to the minimum processing feature size and having slit side walls corresponding to end faces of the two mask portions; forming a second mask layer on the slit sidewalls, thereby reducing the width of the slit; etching the conductive layer using the first and second mask layers to separate the conductive layer into at least two conductive layer portions, the at least two conductive layer portions being separated by a distance which is less than the minimum processing feature size; and ensuring that an area separating the at least two conductive layer portions does not overlap the slit side walls (see Specification at least at p. 16, line 17 through p. 17, line 10; p. 18, lines 5-10; p. 12, line 23 through p. 13, line 2; and FIGs. 6A-6E).

In another aspect of this embodiment, the distance separating the at least two conductive layer portions may be about 1/3 the minimum processing feature size (see Specification at p. 12, lines 16-19 and FIGS. 3E-3F). This dimension ensures that the hole over the gate electrode, for example, is not completely filled by polysilicon 13 (see FIG. 3F).

In another aspect of this embodiment, the method may include contacting a structure underlying the conductive layer through the at least two conductive layer portions (see Specification at p. 16, lines 5-8).

In another aspect of this embodiment the structure underlying the conductive layer has the minimum processing feature size (see Specification at p. 12, lines 5-7).

In another aspect of an embodiment, a method of forming a semiconductor device includes defining an active area in a substrate (see Specification at p. 10, lines 10-16); forming source and drain regions in the active area with a gate structure overlying the substrate therebetween (see Specification at p. 11, lines 15-20); forming a conductive layer over the substrate and the gate structure (see Specification at p. 10, lines 17-19); forming a first mask over the conductive layer (see Specification at p. 11, lines 25-27); performing conventional photolithography to form a slit in a part of the first mask layer overlying the gate structure (see Specification at p. 11, line 28 through p. 12, line 2, and FIG. 3D); forming a second mask layer on the first mask layer and in the slit (see Specification at p. 12, lines 13-16); selectively etching away the second mask layer to leave the second mask layer on side faces of the first mask layer in the slit (see Specification at p. 12, lines 20-22, and FIG. 3G); etching the conductive layer using the first and second mask layers as a mask, thereby patterning the conductive layer into at least two portions separated by a distance which is less than a minimum processing size achievable by the conventional photolithography (see Specification at p. 12, line 28 through p. 13, line 2); and ensuring that an area between the separated at least two portions does not overlap either of the side faces of the first mask layer in the slit (see Specification at p. 8, lines 14-26 and FIG. 3G).

In another aspect, both the first mask layer and the second mask layer may have etch rates slower than an etch rate of the conductive layer (see Specification at p. 14, lines 14-24 and p. 18, lines 11-16). Each of the first mask layer and the second mask layer may be formed from an insulating film (see Specification at p. 14, lines 1-5).

VI. ISSUES

A. Has the Examiner established a *prima facie* case of unpatentability of claims 1-9, 21-32, and 34-39 over Chiu (US 4,994,402), such that these claims are unpatentable under 35 U.S.C. §103(a)?

1. Has the Examiner established that Chiu teaches or suggests all the claimed limitations?

2. Has the Examiner established any motivation or need to modify Chiu in any way such that the rejected claims are unpatentable under §103, and if any motivation to modify Chiu was established, is the motivation to make the modification in the manner suggested proper, given that Chiu specifically teaches against at least one aspect of the claimed invention, and that Chiu does not even acknowledge the technical problem solved by Appellant's claimed invention?

B. Has the Examiner established a *prima facie* case of unpatentability of claims 1-9, 21-32, and 34-39 over Matthews (US 45,134,083), such that these claims are unpatentable under 35 U.S.C. §103(a)?

1. Has the Examiner established that Matthews teaches or suggests all the claimed limitations?

2. Has the Examiner established any motivation or need to modify Matthews in any way such that the rejected claims are unpatentable under §103, and if any motivation to modify Matthews was established, is the motivation to make the modification in the manner suggested proper, given that Matthews does not even acknowledge the technical problem solved by Appellants' claimed invention?

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have not been separately grouped, and thereby stand or fall together.

VIII. ARGUMENTS

A. The Examiner has not established a *prima facie* case of unpatentability under 35 U.S.C. §103(a) of claims 1-9, 21-32, and 34-39 over Chiu (US 4,994,402).

As a preliminary matter, the undersigned notes that the alternative §103 rejections over Chiu ***OR*** Matthews appears not to be in accordance with the MPEP, nor in line with the Office's goal of compact prosecution. The presentation of the statement of the rejections appears to invoke language customarily associated with anticipation rejections under 35 U.S.C. §102, and not unpatentability rejections under 35 U.S.C. §103(a).

Appellant submits that the applied art is not anticipatory, and also that unpatentability under 103(a) has not been established.

1. The Examiner has not established that Chiu teaches or suggests all the claimed limitations.

Appellant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference must teach or suggest all the claim limitations***.[1] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in [Appellant's] disclosure.[2]

Sub-Photolithographic Features are not Taught or Suggested by Chiu

The Examiner appears to have confused disclosure of "dimensions in the submicron range" (Chiu, col. 2, lines 10-20) with Appellant's disclosed and variously claimed features which are smaller than those achievable by conventional photolithographic techniques, i.e., features which are ***sub-photolithographic***.

Appellant submits that the Examiner's assertions regarding submicron dimensions and resolutions are not on point, and are irrelevant to the gist of the disclosed and claimed invention, which relates to ***sub-photolithographic*** features and dimensions, i.e., dimensions which are ***less***

[1] *See* MPEP §2143.
[2] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.

than dimensions conventionally achievable by standard photolithographic techniques. Chiu does not appear to even acknowledge achieving feature sizes less than the conventional photolithographic limit.

Appellant submits that there is a recognized fundamental conceptual difference between dimensions which are less than dimensions achievable by conventional photolithographic techniques, and ***submicron*** dimensions or resolutions. Conventional techniques such as Chiu and Matthews are capable of achieving sub-micron feature sizes, but do not address achieving feature sizes smaller than the conventional limit

Appellant reiterates that submicron size does not equate to sub-photolithographic features or features smaller than those conventionally achievable by photolithographic techniques.

Chiu Does not Teach or Suggest all the Claimed Limitations

Chiu does not teach or suggest a method for manufacturing a semiconductor device wherein the method includes, among other features, "...selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an opening between the second side walls ***smaller than the minimum processing size achievable with the conventional lithographic process technique***...wherein said buried conductive layer includes said second conductive film extending over the gate electrode of the MOS transistor; and ***ensuring that the opening between the second side walls does not overlap either of the first sidewall insulating films or either of the source and drain***", as recited in independent claim 1 (emphasis added).

Chiu does not teach or suggest a method of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size which includes, among other features, "...patterning the first mask layer to form a slit dividing the first mask layer...***having a width equal in size to the minimum processing feature size*** and having slit side walls...forming a second mask layer on the slit sidewalls, thereby reducing the width of the slit;

etching the conductive layer...to separate the conductive layer into at least two conductive layer portions...***separated by a distance which is less than the minimum processing feature size***; and ***ensuring that an area separating the at least two conductive layer portions does not overlap the slit side walls***", as recited in independent claim 21 (emphasis added).

Chiu does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...performing conventional photolithography to form a slit in a part of the first mask layer overlying the gate structure...etching the conductive layer using the first and second mask layers as a mask...patterning the conductive layer into at least two portions ***separated by a distance which is less than a minimum processing size achievable by the conventional photolithography***; and ***ensuring that an area between the separated at least two portions does not overlap either of the side faces of the first mask layer in the slit***", as recited in independent claim 28 (emphasis added).

Chiu does not teach or suggest a method of manufacturing a semiconductor device, which includes, among other features, "...patterning the first layer to have holes with sidewalls separated by a width equal to a minimum feature size achievable by a conventional lithographic process...***forming a second layer on the sidewalls so as to reduce the width of the holes to be less than the minimum feature size***; patterning a conductive layer beneath the first and second layers using the holes ***to form openings in the conductive layer that are smaller in size than the minimum feature size***; and ***ensuring that the holes having the width less than the minimum feature size do not overlap any diffusion region of the semiconductor device***", as recited in independent claim 31, as amended (emphasis added).

Chiu does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...forming a gate electrode overlying the substrate between the source and drain regions, ***the gate electrode having a width no larger than a minimum processing size available with a conventional photolithographic process***...forming a contact hole in the first layer in an area above the gate electrode, ***the contact hole having a width smaller than the minimum processing size of the conventional photolithographic process***; and

ensuring that the contact hole does not overlap either of the source and drain regions", as recited in independent claim 34 (emphasis added).

Chiu does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...forming a structure having a first width on a substrate, ***said first width being a minimum feature size achievable by a conventional lithographic process***...forming slit in the first layer located over the structure, the slit having sidewall spacers separated by a second width, ***wherein the second width is smaller than the minimum feature size achievable with a lithographic process used for making such device***; and ***ensuring that the slit does not overlap an active region of the semiconductor device***", as recited in independent claim 38 (emphasis added).

Chiu does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...defining an active area in a substrate with isolation structures, ***the isolation structures each having a width no larger than a minimum processing size available with a conventional photolithographic process...forming a contact hole in the first layer in an area above the isolation structure...having a width smaller than the minimum processing size of the conventional photolithographic process***; and ***ensuring that the contact hole does not overlap the active area in the substrate***", as recited in independent claim 39 (emphasis added).

Therefore, since the applied art does not teach or suggest all the claimed limitations, reversal of the rejections and allowance of independent claims 1, 21, 28, 31, 34, 38, and 39 are requested. Further, as dependent claims 2-9, 22-27, 29-30, 32, and 35-37 variously and ultimately depend from the allowable independent claims, reversal of the rejections and allowance of these dependent claims are also requested.

2. The Examiner has not established any motivation or need to modify Chiu in any way such that the rejected claims are unpatentable under §103, and even if any motivation to modify Chiu was established, such motivation was improperly based upon hindsight, particularly since Chiu specifically teaches against at least one aspect of the claimed

invention, and further since Chiu does not even acknowledge the technical problem solved by Appellant's claimed invention.

An essential evidentiary component of an obviousness rejection is a teaching or suggestion or motivation to combine the prior art references.[3] Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[4]

"There are three possible sources for a motivation to combine references: ***the nature of the problem to be solved***, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."[5] Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.[6] The level of skill in the art cannot be relied upon to provide the suggestion to combine references.[7]

As indicated above, case law mandates that a *prima facie* case of unpatentability can only be established if there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, ***to modify the reference or to combine reference teachings***. The Final Official Action is silent on any need to modify the applied art, and is also silent on any motivation to modify the applied art.

Chiu is directed to a method of conventional fabrication of a coplanar, self-aligned contact structure in a semiconductor device. Chiu is ***not*** directed to provision of feature sizes or holes having dimensions smaller than that achievable by standard photolithographic techniques. In fact, Chiu does not teach or suggest a solution, and does not even acknowledge the technical problems associated with manufacture of semiconductor devices having sub-photolithographic feature sizes, as in Appellant's disclosed and claimed invention.

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[3] *C.R. Bard, Inc. v. M3 Systems, Inc.*, 48 USPQ2d 1225 (Fed. Cir. 1998)
[4] *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)
[5] *See* MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).
[6] *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).
[7] *See* MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).

As indicated above, there is no indication in the Official Action of any need to modify or combine any aspect of Chiu, and there is no statement provided by the Examiner regarding any claimed limitation which is asserted as not being explicitly present in the reference, such that any modification would be necessary.

Further, the Examiner's rationale for making the statement in the Final Official Action is unclear. This statement notes that "Chiu and Matthews may have additional steps in their process, however the instant claims include the term 'comprising' that does not exclude additional steps and further current case law states: As a matter of fact selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results...."[8]

The fact that the transition term "comprising" is used in the instant claims is suggested as not being relevant with respect to the deficiencies noted in the applied art, as discussed above. Whether or not the applied art *may have* additional steps is irrelevant to the claimed invention; is Appellant submits that what is relevant is that the applied art does not teach or suggest all the limitations explicitly recited in the claims on appeal.

Appellant notes that the case cited by the Examiner, *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946), also cited in MPEP §2144.04, stands for the proposition that the selection of a different order of performing process steps is *prima facie* obvious without a showing of new or unexpected results.

However, Appellant has yet not explicitly claimed any required order of the steps, thus raising a question of the purpose of this case citation by the Examiner, and its bearing on establishment of a *prima facie* case of unpatentability with respect to the applied art.

Therefore, Appellants submit that, at least for these reasons, the Examiner has failed to meet his threshold burden in establishing a *prima facie* case of unpatentability of the pending claims. Reversal of the unpatentability rejections and allowance of claims 1-9, 21-32, and 34-39 are requested.

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[8] *See* Final Official Action at p. 5.

Chiu Teaches Away from at Least One Aspect of Appellant's Claimed Invention

It is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art.[9] Further in this regard, As the Court of Customs and Patent Appeals, predecessor to the Federal Circuit, has held:

> All relevant teachings of cited references must be considered in determining what they fairly teach to one having ordinary skill in the art. The relevant portions of a reference include not only those teachings which would suggest particular aspects of an invention to one having ordinary skill in the art, but also those teachings which would lead such a person away from the claimed invention.[10]

Chiu teaches away from at least one aspect of Appellant's disclosed and claimed invention, by stating unequivocally that hole alignment is not critical.

In particular, Chiu teaches:

> ***[N]o ill effects are suffered if one of the holes is wider than the pad*** which lies beneath it or slightly misaligned with respect thereto. Accordingly, one or both holes can ***intentionally*** be made wider than the underlying pads if desired.[11]

This teaching of no ill effects of misalignment, and the further teaching in Chiu FIG. 14 regarding the alignment of holes 99 and 101 directly over the sidewall of pads 49 and 51 is ***directly contrary*** to at least one claimed objective of Appellant's disclosed and variously claimed invention, i.e., to ensure that the narrow contact hole does ***not*** overlap an active region of the device or an underlying sidewall region.

This teaching of Chiu is closely comparable to the undesirable aspects of Appellant's prior art illustrated in FIG. 2, resulting, in some circumstances, in etching of the undesirable

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[9] *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 230 USPQ 416 (Fed. Cir. 1986).
[10] *In re Mercier*, 185 USPQ 774, 778 (CCPA 1975).
[11] *See* Chiu at col. 7, lines 50-55 (emphasis added).

trench 120 in substrate 101 and/or diffusion layers 106 or 109.

In particular, independent claim 1, as amended, recites a method for manufacturing a semiconductor device which includes, among other limitations, "...***ensuring that the opening between the second side walls does not overlap either of the first sidewall insulating films or either of the source and drain***."

Thus, Appellant submits that a person having skill in the art would not be motivated to rely upon the teachings of Chiu to solve the technical problem addressed by Appellant's disclosed and claimed invention because Chiu does not regard alignment of the contact hole above the sidewall as a problem. Therefore, Appellant submits that any motivation to modify Chiu is based upon impermissible hindsight analysis, because Chiu is not properly modifiable by itself or combinable with any other reference for the purposes of rendering obvious Appellant's recited invention at least in light of the aspect of Chiu which teaches away from the claimed invention.

Chiu Does not Acknowledge the Technical Problems Solved

As discussed in the case law above, one of the three possible sources for a motivation to combine references is the nature of the technical problem to be solved.

As described in the Summary of the Invention section of this Brief, Appellant's disclosed and claimed invention is directed to a method for manufacturing a semiconductor device which has a buried conductive layer connected, in one embodiment, to a source or drain of a MOS transistor through a contact hole having dimensions smaller than that achievable solely by reliance upon available photolithographic processing limits. Further, in view of the sub-photolithographic feature sizes achievable by the recited method, the method of Appellant's invention is designed so as to ensure that the contact hole avoids undesirable and detrimental alignment with an associated sidewall below the contact hole, e.g., sidewalls on a gate structure, and instead generally aligns with a central portion of the underlying device element.

One technical problem solved by Appellant's recited invention is to prevent damage to the silicon substrate due to exposure resulting from the undesirable alignment of the contact hole with the underlying sidewall below the contact hole. Prevention of damage to the underlying substrate, for example, is accomplished by ensuring that the contact hole is narrower than an underlying gate length, and is sufficiently centered above the gate structure so as to avoid registration or overlap with any associated sidewall underneath the contact hole.

Therefore, Appellants again submit that a person of ordinary skill in the art would not be motivated to modify or combine Chiu with any other reference, such that the unpatentability rejections of the pending claims should be reversed.

B. The Examiner has not established a *prima facie* case of unpatentability under 35 U.S.C. §103(a) of claims 1-9, 21-32, and 34-39 over Matthews (US 45,134,083).

Citations to case law regarding unpatentability under 35 U.S.C. §103(a) has been provided above.

1. The Examiner has not established that Matthews teaches or suggests all the claimed limitations.

Reiterating the remarks made above with respect to Chiu, the Examiner appears to have confused disclosure of "sub-micron resolutions" (Matthews, col. 1, lines 42-47) with Appellant's disclosed and variously claimed ***sub-photolithographic*** features which are smaller than those achievable by conventional photolithographic techniques. Submicron resolutions do not equate to sub-photolithographic features or features smaller than those conventionally achievable by photolithographic techniques.

Matthews Does not Teach or Suggest all the Claimed Limitations

Matthews does not teach or suggest a method for manufacturing a semiconductor device wherein the method includes, among other features, "...selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process

said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an opening between the second side walls ***smaller than the minimum processing size achievable with the conventional lithographic process technique***...wherein said buried conductive layer includes said second conductive film extending over the gate electrode of the MOS transistor; and ***ensuring that the opening between the second side walls does not overlap either of the first sidewall insulating films or either of the source and drain***", as recited in independent claim 1 (emphasis added).

Matthews does not teach or suggest a method of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size which includes, among other features, "...patterning the first mask layer to form a slit dividing the first mask layer...***having a width equal in size to the minimum processing feature size*** and having slit side walls...forming a second mask layer on the slit sidewalls, thereby reducing the width of the slit; etching the conductive layer...to separate the conductive layer into at least two conductive layer portions...***separated by a distance which is less than the minimum processing feature size***; and ***ensuring that an area separating the at least two conductive layer portions does not overlap the slit side walls***", as recited in independent claim 21 (emphasis added).

Matthews does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...performing conventional photolithography to form a slit in a part of the first mask layer overlying the gate structure...etching the conductive layer using the first and second mask layers as a mask...patterning the conductive layer into at least two portions ***separated by a distance which is less than a minimum processing size achievable by the conventional photolithography***; and ***ensuring that an area between the separated at least two portions does not overlap either of the side faces of the first mask layer in the slit***", as recited in independent claim 28 (emphasis added).

Matthews does not teach or suggest a method of manufacturing a semiconductor device, which includes, among other features, "...patterning the first layer to have holes with sidewalls separated by a width equal to a minimum feature size achievable by a conventional lithographic process...***forming a second layer on the sidewalls so as to reduce the width of the holes to be***

less than the minimum feature size; patterning a conductive layer beneath the first and second layers using the holes ***to form openings in the conductive layer that are smaller in size than the minimum feature size***; and ***ensuring that the holes having the width less than the minimum feature size do not overlap any diffusion region of the semiconductor device***", as recited in independent claim 31 (emphasis added).

Matthews does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...forming a gate electrode overlying the substrate between the source and drain regions, ***the gate electrode having a width no larger than a minimum processing size available with a conventional photolithographic process***...forming a contact hole in the first layer in an area above the gate electrode, ***the contact hole having a width smaller than the minimum processing size of the conventional photolithographic process***; and ***ensuring that the contact hole does not overlap either of the source and drain regions***", as recited in independent claim 34 (emphasis added).

Matthews does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...forming a structure having a first width on a substrate, ***said first width being a minimum feature size achievable by a conventional lithographic process***...forming slit in the first layer located over the structure, the slit having sidewall spacers separated by a second width, ***wherein the second width is smaller than the minimum feature size achievable with a lithographic process used for making such device***; and ***ensuring that the slit does not overlap an active region of the semiconductor device***", as recited in independent claim 38 (emphasis added).

Finally, Matthews does not teach or suggest a method of forming a semiconductor device which includes, among other features, "...defining an active area in a substrate with isolation structures, ***the isolation structures each having a width no larger than a minimum processing size available with a conventional photolithographic process...forming a contact hole in the first layer in an area above the isolation structure...having a width smaller than the minimum processing size of the conventional photolithographic process***; and ***ensuring that the contact***

hole does not overlap the active area in the substrate", as recited in independent claim 39 (emphasis added).

2. The Examiner has not established any motivation or need to modify Matthews in any way such that the rejected claims are unpatentable under §103, and even if any motivation to modify Matthews was established, such motivation was improperly based upon hindsight, particularly since Matthews does not even acknowledge the technical problem solved by Appellant's claimed invention.

Matthews is directed to processes for simultaneously fabricating CMOS and bipolar transistors (i.e., "BiCMOS" devices) in the same semiconductor device. Matthews, similar to Chiu, does not acknowledge the technical problem solved by Appellant's disclosed and claimed invention relating to provision of ***sub-photolithographic feature sizes*** in a semiconductor device.

For example, Matthews at col. 1, lines 44-47, indicates that "state-of-the-art optics, projection printing...systems are capable of producing sub-micron resolutions." This existing conventionally achievableresolution is used in the invention of Matthews to form BiCMOS devices with improved dimensions and densities, owing, at least in part, to Matthews inventive method which uses high levels of planarization throughout wafer processing by a so-called "waffelization" technique.[12]

As indicated above, case law mandates that a *prima facie* case of unpatentability can only be established if there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, ***to modify the reference or to combine reference teachings***.

There is no indication in the Official Action of any need to modify or combine any aspect of Matthews, and there is no statement provided by the Examiner regarding any claimed limitation which is asserted as not being explicitly present in the applied art, such that modification would be required. The Final Official Action is absolutely silent on this point.

[12] *See* Matthews at least at col. 2, lines 35-59.

Thus, Appellant submits that, even assuming, *arguendo* that Matthews taught or suggested all the claimed limitations, a person having skill in the art would not be motivated to rely upon the teachings of Matthews to solve the technical problem addressed by Appellant's disclosed and claimed invention. Therefore, Matthews is submitted as not being properly modifiable on its own, for the purposes of rendering obvious Appellant's recited invention.

The Boards' attention is invited to *In re Kotzab*, wherein the CAFC held that, even when various elements of the claimed invention were present (in two separate embodiments of the same prior art reference), if there was no motivation to combine the elements from the separate embodiments of the single reference, based on the teachings in the prior art, then an unpatentability rejection can not be upheld.[13]

Appellant submits that, in the instant appeal, there is not even the presence of the recited limitation in any embodiment of Matthews. Therefore, Appellants submit that the Examiner has again failed to meet his threshold burden in establishing a *prima facie* case of unpatentability of the pending claims. Reversal of the unpatentability rejections and allowance of the claims on appeal are requested.

Matthews Does not Acknowledge the Technical Problems Solved

Appellant's disclosed and claimed invention is directed to a method for manufacturing a semiconductor device which has a buried conductive layer connected, in one embodiment, to a source or drain of a MOS transistor through a contact hole ***having dimensions smaller than that achievable solely by reliance upon available photolithographic processing limits***. Further, in view of the sub-photolithographic feature sizes achievable by the recited method, the method of Appellant's invention is designed so as to ensure that the contact hole avoids undesirable and detrimental alignment with an associated sidewall below the contact hole, e.g., sidewalls on a gate structure, and instead generally aligns with a central portion of the device element.

[13] *In re Kotzab*, 55 USPQ2d 1313 (Fed. Cir. 2000).

As previously discussed, one technical problem solved by Appellant's recited invention is to prevent damage to the silicon substrate due to exposure resulting from the undesirable alignment of the contact hole with the underlying sidewall below the contact hole. Prevention of damage to the underlying substrate, for example, is accomplished by ensuring that the contact hole is, in one embodiment, narrower than an underlying gate length, and is sufficiently centered above the gate structure so as to avoid registration or overlap with any associated sidewall underneath the contact hole.

This problem is not even acknowledged by Matthews. Therefore, Appellants submit that a person of ordinary skill in the art would not be motivated to modify or combine Matthews, absent some suggestion to do so in the applied art. The applied art is silent in this regard, and the Examiner has not met his burden in establishing a *prima facie* case of unpatentability under §103(a).

Accordingly, for the various reasons set forth above, reversal of the unpatentability rejections and allowance of claims 1-9, 21-32, and 34-39 by the Honorable Board are requested.

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Appellant on October 16, 2003.

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/008,497

1. A method for manufacturing a semiconductor device having a buried conductive layer which is connected to one of a source and a drain of a MOS transistor and which extends over a gate electrode of said MOS transistor, said method comprising:

forming a first insulating film on a semiconductor substrate;

forming a first conductive film as said gate electrode and a second insulating film on said first insulating film, said gate electrode having a width equal to a minimum processing size achievable with a conventional lithographic process technique;

forming a third insulating film on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film and said second insulating film formed thereon;

selectively etching away said third insulating film so as to form first side wall insulating films including said third insulating film on each of both side faces of said first conductive film and said second insulating film,

said selective etching exposing said semiconductor substrate in portions which are not covered with said side wall insulating film and not covered with said first conductive film;

diffusing impurities into said exposed portions of said semiconductor substrate so as to form a source and a drain in said semiconductor substrate;

forming a second conductive film to be a part of said buried conductive layer on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film and said side wall insulating film formed thereon;

forming a first mask layer on said second conductive film;

processing said first mask layer to have a pattern which is separated into both side portions as to said first conductive film;

forming a second mask layer on the whole surface of said semiconductor substrate having

said first insulating film, said first conductive film, said second insulating film, said side wall insulating film, said second conductive film and said first mask layer formed thereon;

selectively etching away said second mask layer so as to leave a pattern of said second mask layer as second side walls on each of both side faces of the pattern of said first mask layer;

selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an opening between the second side walls smaller than the minimum processing size achievable with the conventional lithographic process technique, and

wherein said buried conductive layer includes said second conductive film extending over the gate electrode of the MOS transistor; and

ensuring that the opening between the second side walls does not overlap either of the first sidewall insulating films or either of the source and drain.

2. A method for manufacturing a semiconductor device according to claim 1, wherein said first mask layer is formed of an insulating film, and said second mask layer is formed of a conductive film.

3. A method for manufacturing a semiconductor device according to claim 1, wherein each of said first and second mask layers is formed of an insulating film.

4. A method for manufacturing a semiconductor device according to claim 1, wherein said first mask layer is formed of a conductive film, and said second mask layer is formed of an insulating film.

5. A method for manufacturing a semiconductor device according to claim 1, wherein each of said first and second mask layers is formed of a conductive film.

6. A method for manufacturing a semiconductor device according to claim 1, further comprising the steps of:

forming, after said step of selectively etching away said second conductive film, an interlayer insulating film on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film, said side wall insulating film, said second conductive film, and said first and second mask layers formed thereon;

forming a contact hole through both said interlayer insulating film and said first mask layer so that said contact hole reaches said second conductive film; and

forming a wiring layer which is connected to said second conductive film at the bottom of said contact hole.

7. A method for manufacturing a semiconductor device according to claim 1, further comprising the steps of:

forming, after said step of selectively etching away said second conductive film, a fourth insulating film on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film, said side wall insulating film, said second conductive film, and said first and second mask layers formed thereon;

forming a contact hole through both said fourth insulating film and said first mask layer so that said contact hole reaches said second conductive film;

forming a third conductive film in the inside of said contact hole so that said third conductive film reaches said second conductive film;

processing said third conductive film into an electrode pattern;

coating a surface of said third conductive film, which has been processed into the electrode pattern, with a dielectric film;

forming a fourth conductive film on said dielectric film; and

processing said fourth conductive film into an electrode pattern.

8. A method for manufacturing a semiconductor device according to claim 1, further comprising the steps of:

removing said first mask layer after said step of selectively etching away said second conductive film;

coating at least a surface of said second conductive film with a dielectric film;

forming a third conductive film on said dielectric film; and

processing said third conductive film into an electrode pattern.

9. A method for manufacturing a semiconductor device according to claim 8 further comprising the step of coating a surface of said second mask layer with a dielectric film.

21. A method of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size, comprising:

forming a semiconductor element in a substrate;

forming a conductive layer over the semiconductor element and the substrate;

forming a first mask layer on the conductive layer;

patterning the first mask layer to form a slit dividing the first mask layer into at least two mask portions, the slit having a width equal in size to the minimum processing feature size and having slit side walls corresponding to end faces of the two mask portions;

forming a second mask layer on the slit sidewalls, thereby reducing the width of the slit;

etching the conductive layer using the first and second mask layers to separate the conductive layer into at least two conductive layer portions, the at least two conductive layer portions being separated by a distance which is less than the minimum processing feature size; and

ensuring that an area separating the at least two conductive layer portions does not overlap the slit side walls.

22. The method of claim 21 wherein the distance separating the at least two conductive layer portions is about 1/3 the minimum processing feature size.

23. The method of claim 21 further comprising contacting a structure underlying the conductive layer through the at least two conductive layer portions.

24. The method of claim 23 wherein the structure underlying the conductive layer has the minimum processing feature size.

25. The method of claim 21 wherein each of the first mask layer and second mask layer is formed from an insulating film.

26. The method of claim 21 wherein the first mask layer is formed from a conductive film and the second mask layer is formed from an insulating film.

27. The method of claim 21 wherein each of the first mask layer and second mask layer is formed from a conductive film.

28. A method of forming a semiconductor device, comprising:

defining an active area in a substrate;

forming source and drain regions in the active area with a gate structure overlying the substrate therebetween;

forming a conductive layer over the substrate and the gate structure;

forming a first mask over the conductive layer;

performing conventional photolithography to form a slit in a part of the first mask layer overlying the gate structure;

forming a second mask layer on the first mask layer and in the slit;

selectively etching away the second mask layer to leave the second mask layer on side faces of the first mask layer in the slit;

etching the conductive layer using the first and second mask layers as a mask, thereby patterning the conductive layer into at least two portions separated by a distance which is less than a minimum processing size achievable by the conventional photolithography; and

ensuring that an area between the separated at least two portions does not overlap either of the side faces of the first mask layer in the slit.

29. The method of claim 28 wherein both the first mask layer and the second mask layer have etch rates slower than an etch rate of the conductive layer.

30. The method of claim 28 wherein each of the first mask layer and the second mask layer are formed from an insulating film.

31. A method of manufacturing a semiconductor device, the method comprising:

forming a first layer over a semiconductor substrate;

patterning the first layer to have holes with sidewalls separated by a width equal to a minimum feature size achievable by a conventional lithographic process used during manufacture of the device;

forming a second layer on the sidewalls so as to reduce the width of the holes to be less than the minimum feature size;

patterning a conductive layer beneath the first and second layers using the holes to form openings in the conductive layer that are smaller in size than the minimum feature size; and

ensuring that the holes having the width less than the minimum feature size do not overlap any diffusion region of the semiconductor device.

32. The method of claim 31 wherein the first layer and the second mask layer have etch rates slower than an etch rate of the conductive layer.

34. A method of forming a semiconductor device, comprising:

defining an active area in a substrate;

forming source and drain regions in the active area;

forming a gate electrode overlying the substrate between the source and drain regions, the gate electrode having a width no larger than a minimum processing size available with a conventional photolithographic process associated with forming the gate electrode;

forming a first layer over at least the active area of the substrate;

forming a contact hole in the first layer in an area above the gate electrode, the contact hole having a width smaller than the minimum processing size of the conventional photolithographic process; and

ensuring that the contact hole does not overlap either of the source and drain regions.

35. The method of claim 34 further comprising contacting the gate electrode through the contact hole.

36. The method of claim 34 wherein forming the contact hole comprises:

forming a first mask on the first layer;

patterning the first mask to form a slit dividing the first mask into at least two mask portions, the slit having a width equal in size to the minimum processing feature size and having side walls corresponding to end faces of the two mask portions;

forming a second mask on the slit sidewalls, thereby reducing the width of the slit; and

etching the first layer using the first and second mask to form the contact hole.

37. The method of claim 36 wherein forming the second mask comprises:

forming a second mask layer on the first mask and in the slit; and

selectively etching away the second mask to leave the second mask on side walls of the first mask in the slit.

38. A method of forming a semiconductor device, comprising:

forming a structure having a first width on a substrate, said first width being a minimum feature size achievable by a conventional lithographic process;

forming a first layer over at least the structure; and

forming slit in the first layer located over the structure, the slit having sidewall spacers separated by a second width,

wherein the second width is smaller than the minimum feature size achievable with a lithographic process used for making such device; and

ensuring that the slit does not overlap an active region of the semiconductor device.

39. A method of forming a semiconductor device, comprising:

defining an active area in a substrate with isolation structures, the isolation structures each having a width no larger than a minimum processing size available with a conventional photolithographic process associated with forming the isolation structure;

forming a first layer over at least the isolation structure;

forming a contact hole in the first layer in an area above the isolation structure, the contact hole having a width smaller than the minimum processing size of the conventional photolithographic process; and

ensuring that the contact hole does not overlap the active area in the substrate.